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DATE: Thursday, January 29, 2004

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		DB=USPT; PLUR=NO; OP=ADJ	
☐	L5	L4 not l3	14
☐	L4	intel.asn. and L1	26
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☐	L1	memory controller$1 and input/output controller$1	347

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L2: Entry 40 of 58 File: USPT Jul 4, 1995

US-PAT-NO: 5430641
DOCUMENT-IDENTIFIER: US 5430641 A

TITLE: Synchronously switching inverter and regulator

DATE-ISSUED: July 4, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kates; Barry K.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dell USA, L.P.	Austin	TX			02

APPL-NO: 08/ 192944 [PALM]
DATE FILED: February 7, 1994

PARENT-CASE:
This is a continuation of application Ser. No. 07/874,482, filed Apr. 27, 1992, now abandoned.

INT-CL: [06] H02 M 7/538

US-CL-ISSUED: 363/133; 363/23, 363/97, 363/124, 323/266
US-CL-CURRENT: 363/133; 323/266, 363/124, 363/23, 363/97

FIELD-OF-SEARCH: 323/222, 323/232, 323/266, 323/272, 323/282, 363/22, 363/23, 363/24, 363/25, 363/26, 363/65, 363/71, 363/97, 363/133, 363/134

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3742330	June 1973	Hodges et al.	323/266
☐	4034280	July 1977	Cronin et al.	363/97
☐	4095128	June 1978	Tanigaki	307/254
☐	4251857	February 1981	Shelly	363/124
☐	4661896	April 1987	Kobayashi et al.	323/266

☐	4725768	February 1988	Watanabe	323/222
☐	4905136	February 1990	Tanaka	363/124
☐	5070439	December 1991	Remson	363/22
☐	5138249	August 1992	Capel	363/124
☐	5162981	November 1992	Lazar et al.	363/22

ART-UNIT: 212

PRIMARY-EXAMINER: Sterrett; Jeffrey L.

ATTY-AGENT-FIRM: Huffman; James Hoop; Jeff

ABSTRACT:

Synchronous switching inverter and regulator suppress rf emissions, and FET push-pull switching for the inverter provides high efficiency power transfer by sinusoidal transformer operation. Feedback control for both pass transistors switching and duty cycles insures overall synchronous behavior.

12 Claims, 21 Drawing figures

L2: Entry 40 of 58 File: USPT Jul 4, 1995

DOCUMENT-IDENTIFIER: US 5430641 A
TITLE: Synchronously switching inverter and regulator

Detailed Description Text (3):
FIG. 3A is a schematic block diagram of a first preferred embodiment portable computer system which includes microprocessor 300, bus and memory controller 310, bus 311, memory 312, power consumption management 320, video controller 330, hard disk drive 340, and input/output controller 350.

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L5: Entry 8 of 14 File: USPT Jun 4, 2002

US-PAT-NO: 6401208
DOCUMENT-IDENTIFIER: US 6401208 B2

TITLE: Method for BIOS authentication prior to BIOS execution

DATE-ISSUED: June 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; Derek L.	Phoenix	AZ		
Mehta; Pranav	Chandler	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 118147 [PALM]
DATE FILED: July 17, 1998

INT-CL: [07] H04 L 9/32, G06 F 12/14, G06 F 11/30

US-CL-ISSUED: 713/193; 713/189, 713/188, 713/187, 713/191
US-CL-CURRENT: 713/193; 713/187, 713/188, 713/189, 713/191

FIELD-OF-SEARCH: 713/187-188, 713/189, 713/191, 713/193, 713/200

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5022077	June 1991	Bealkowski et al.	
☐	5276853	January 1994	Yamaguchi et al.	711/131
☐	5421006	May 1995	Jablon et al.	714/36
☐	5444850	August 1995	Chang	709/222
☐	5473692	December 1995	Davis	
☐	5539828	July 1996	Davis	
☐	5568552	October 1996	Davis	
☐	5796840	August 1998	Davis	

☐	5805712	September 1998	Davis	
☐	5828753	October 1998	Davis	
☐	5835594	November 1998	Albrecht et al.	713/187
☐	5844986	December 1998	Davis	713/187
☐	5919257	July 1999	Trostle	713/200
☐	6009524	December 1999	Olarig et al.	713/200
☐	6061794	May 2000	Angelo et al.	713/200

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
WO 98/15082	April 1998	WO	

OTHER PUBLICATIONS

Lynch, "CSC 277--Operating Systems," Jul. 2000, http://www.qvctc.commnet.edu/classes/csc277/bios.hml [internet].*
"Windows 2000 Professional Intel-based boot process," http://www.gateway.com/sup..roduct/software/win2000/750433034.shtml [internet]Jul. 2000.

ART-UNIT: 2767

PRIMARY-EXAMINER: Decady; Albert

ASSISTANT-EXAMINER: Kabakoff; Steve

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

A cryptographic device is implemented in communication with a host processor to prevent the host processor from performing a standard boot-up procedure until a basic input output system (BIOS) code is authenticated. This is accomplished by a cryptographic device which is addressed by the host processor during execution of a first instruction following a power-up reset. The cryptographic device includes a first integrated circuit (IC) device and a second IC device. The first IC device includes a memory to contain firmware and a root certification key. The second IC device includes logic circuitry to execute a software code to authenticate the BIOS code before permitting execution of the BIOS code by the host processor.

19 Claims, 7 Drawing figures

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L5: Entry 8 of 14 File: USPT Jun 4, 2002

DOCUMENT-IDENTIFIER: US 6401208 B2
TITLE: Method for BIOS authentication prior to BIOS execution

Assignee Name (1):
Intel Corporation

Detailed Description Text (20):
In order to maintain compatibility with legacy memory controller hub and I/O controller hub devices, this data cycle is configured to appear as an instruction fetch cycle. This is accomplished by placing the host processor into a CHECK mode by setting an opcode fetch emulation bit. Herein, the architecture of the host processor includes the opcode fetch emulation bit that defaults to a "SET" state after a power-on reset. Upon detecting that the opcode fetch emulation bit is set, the host processor deasserts a data/control (D/C#) control line so that the data fetch appears to the chipset as an instruction fetch.

CLAIMS:

1. A system comprising:

a chipset including a controller;

a storage device coupled to the chipset and controlled by the memory controller, the storage device including software code, a digital signature of the software code, and a digital certificate pre-stored within the storage device;

a processor coupled to the chipset via a data/control control line, the processor including an opcode fetch emulation bit, the opcode fetch emulation bit to default to a predetermined state during a power-on reset condition and cause the processor to disguise a data fetch to the storage device as an instruction fetch through deassertion of the data/control control line so that the data fetch appears as an instruction fetch to the controller; and

a cryptographic device in communication with the processor, the cryptographic device to authenticate the software code, loaded into the cryptographic device during a boot procedure, before permitting the processor to execute the software code.

5. The system of claim 1, wherein the controller includes one of a legacy memory control hub device and a legacy input/output controller hub device.